

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) ~~Am~~ A debug and emulation system
2 comprising:

3 a target device embodied in a single integrated circuit
4 including

5 ~~am~~ a function clock circuit generating ~~am~~ a function
6 clock;

7 an operation circuit connected to said function clock
8 circuit operating in synchronism with said function clock;

9 a trace trigger circuit connected to said function clock
10 circuit and said operation circuit, said trace trigger circuit
11 triggering trace of operation of said operation circuit upon
12 detection of a predetermined condition within said operation
13 circuit;

14 a reference clock input for receiving a reference clock
15 signal;

16 a clock circuit connected to said function clock circuit
17 for receiving said function clock signal and to said reference
18 clock input for receiving said reference clock signal, said
19 clock circuit generating an oscillator clock signal
20 synchronous with one of said function clock circuit and said
21 reference clock signal;

22 a trace first-in-first-out buffer having an input
23 connected to said function clock circuit and said operation
24 circuit for storing trace data in synchronism with said
25 function clock signal and an output connected to said ~~phase~~
26 ~~locked-loop~~ clock circuit for outputting trace data in
27 synchronism with said oscillator clock signal; and

28 a trace output port connected to said output of said
29 trace first-in-first-out buffer outputting trace data from
30 said target device; and
31 an emulator connected to said trace output port for sensing
32 said trace data in synchronism with said oscillator clock signal.

1 2. (Original) The debug and emulation system of claim 1,
2 wherein:

3 said emulator includes

4 a reference clock generator connected to said reference
5 clock input for generating said reference clock signal; and

6 a clock control circuit connected to said clock circuit
7 of said target device for controlling whether said oscillator
8 clock signal is synchronous with said function clock circuit
9 or with said reference clock signal.